Notice of Allowability	Application No.	Applicant(s)	
	10/043,237	DOUMAE, YASUHIRO	
	Examin r	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/26/2004*.

2. ☒ The allowed claim(s) is/are *3 – 6, 9 –12 and 15 – 25*.

3. ☒ The drawings filed on *14 January 2002* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachm nt(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *5/24/04*.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowanc
9. ☐ Other _____.

Detailed Action

1. This action is in response to applicant's amendment of 3/26/2004.

Allowed Subject Matter

2. Claims 3 – 6, 9 –12 and 15 – 25 are allowed.

3. Wu (US 5,837,588) teaches (Figures 3 – 7) a method of manufacturing a transistor comprising: a dielectric film on the main surface; forming a conductor layer on the dielectric film; forming a gate electrode by using at least three different masks and etching processes; forming pocket regions in the substrate after using the using the three different masks and etching processes; and forming a source and drain in the main surface.

Claims 3 – 6, 9 -12 and 15 - 22

The prior art does not teach or fairly suggest in combination with the other claimed limitations, a method of manufacturing a field effect transistor having a semiconductor substrate with a main surface comprising: forming a conductive layer on a dielectric film; forming pocket regions in the semiconductor substrate by implanting ions using the single mask; forming a gate electrode by etching the conductive layer using the single mask formed thereon; and wherein the single mask has a width less than a desired width necessary to define a gate length of the gate electrode.

Claims 23 – 25

A method of manufacturing a field effect transistor which comprises the following:

forming a conductive layer over a substrate; forming a single etching mask on the conductive layer; implanting ions through the conductive layer into the substrate and into the substrate under the single etching mask; using the single mask, removing portions of the conductive layer that have been exposed to ion implantation in order to form a gate electrode; forming side walls on the gate electrode; and implanting ions into the substrate using the gate electrode, including the side walls as a mask, to form source and drain regions.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Han et al. (US 5,409,848) teaches an angled pocket implantation semiconductor device.

Tran et al. (US 2002/0068395 A1) teaches a double LDD device.

Wierzorek et al. (US 6,352,885) teaches a transistor having a increased gate insulation.

Dawson (US 6,087,706) teaches a compact transistor structure.

"A Novel Self-aligned Gate-overlapped LDD Poly-Si TFT with High Reliability and Performance", published in the IEEE in 1977 and authored by Mutsuko Hatano, Hajime Akimoto and Takeshi Sakai.

Reber (US 2003/0075806) teaches an integrated circuit having an interconnect to a circuit.

Michael (US 5,869,378) teaches a method of reducing overlap between gate electrodes.

Jecmen (US 4,198,250) teaches a shadow masking process.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl White, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2813

May 25, 2004

Tuan H. Nguyen
Primary Examiner